1. **REFERENCES**

416 Series Order Wire Technical System Description
0416-4602/285 Wiring Diagram, 2 Sheets

2. **DESCRIPTION**

2.1. The -602/285 Order Wire configuration consists of the basic 416 System, with the addition of a 41662 Multi-Channel DTMF Address Decoder and a 41687 Multi-Channel Interface module for two channel capability. The two 4-wire ports have balanced inputs and outputs and are available on the rear panel terminal strips. This configuration also allows one or two 4W/4W or 6W/4W Bridges to be installed. The two Bridges function as stand alone units with all their ports available on the rear panel terminal strips.

2.2. The 41687 Multi-Channel Interface module provides a switchable connection between the Order Wire RCV/XMT port and the two 4-wire ports. Amplifiers on the 41687 module provide impedance conditioning as well as variable gain for level control. Dedicated push-on/push-off switches located on the front panel control channel selection. The channel selector switches are equipped with LEDs which provide visual indications of the associated channel's status (flashing for incoming call, illuminated for channel selected, and extinguished for channel idle). Since each channel has independent control/status indication, it is possible to select none, both, or either one of the channels at one time.

2.3. The 41662 Multi-Channel Address Decoder provides independent DTMF detection and decoding for the two channels. Outputs include a correct address indication and two ringback/LED drivers. The ringback signal is also used to flash the LEDs in the channel selector switches for incoming call indication.

2.4. The 41685 4W/4W (or 41685-01 6W/4W Bridge) is an active conference bridge with 25 dB of through path adjustment available. Amplifiers with potentiometer level adjustment are provided on each input and output for easy level coordination between ports. Transformer coupled inputs and outputs provide DC isolation as well as excellent common-mode rejection.

3. **SIGNAL FLOW**

3.1. The signal flow through the 41651 Transmit and 41650 Receive modules is described by the 416 Series Order Wire Technical System Description.

3.2. TRANSMIT PATH

3.2.1. The output of the 41651 Transmit module (XMT test jack) is routed to the OW XMT INPUT of the 41687 Multi-Channel Interface module. The 41687 module utilizes solid state analog switches to provide line selection capability. Order Wire signals are routed to the appropriate XMT port only when the channel is selected. When the channel is not selected, the isolation is >60 dB.

3.2.2. Channel 1 XMT connects to terminals A1 & A2 on the rear panel. Channel 2 XMT connects to terminals A3 & A4 on the rear panel.

3.3. RECEIVE PATH

3.3.1. Channel 1 RCV(terminals B1 & B2) & CH2 RCV (terminals B3 & B4) are routed to the appropriate RCV port on the 41687 module.

3.3.2. When a channel is selected, signals present at the appropriate RCV port are routed through the 41687 module to its OW RCV OUTPUT. When the channel is not selected, the isolation is >60 dB. The OW RCV OUTPUT of the 41687 module is routed to the input of the 41650 Receive module (RCV test jack).

3.4. AUXILIARY BRIDGES

3.4.1. All ports of the Bridges in J2 and J3 are wired to the rear panel for maximum flexibility in various applications. Each Bridge functions as a conference bridge; i.e. a signal on any LEG input is routed to all the LEG outputs except its own, and a LEG output will include signals from all LEG inputs except its own.

4. INSTALLATION

4.1. Refer to Table B and wiring diagram 0416-4602/285 for the required rear panel terminal strip connections for system operation. If the Bridge(s) are utilized in the Order Wire XMT/RCV path, the connections must be made on the rear panel terminal strips as follows: CH1 (or CH2) XMT to LEG 1 IN and CH1 (or CH2) RCV to LEG 1 OUT.

4.2. The terminal strips are designed to make a crimp connection on the wire when the screw is tightened. To properly utilize this feature, be sure that the wire is placed between the top plate (which comes loose with the screw) and the bottom plate (which is attached to the phenolic material). Do not over tighten the screw. Crimp-on lugs are not used.

4.3. The Order Wire is shipped with the mounting flanges positioned for a 19-inch rack. If the Order Wire is to be installed in a 23-inch rack, remove the flanges and reverse their orientation to accommodate the 23-inch rack. Flanges are also available for ETSI racks.

5. ALIGNMENT

5.1. Alignment of the Order Wire has been performed at the factory. Upon installation the levels should be verified and adjusted as required. Attachment A lists all levels, impedances, etc. for the -602/285 system configuration.

NOTE: *Caution must be exercised during level alignment to insure that proper test levels and impedances are maintained.*

A signal generator may double terminate a port causing a reduced signal level. When injecting a test tone into a port, bridge the port with an AC voltmeter and set the signal generator output according to the AC voltmeter reading.

When taking output level readings, the AC voltmeter will be either terminated or bridged. When it is unknown if an output reading should be a terminated or bridged measurement, compare the two readings. If a 3.5 dB difference is noted, the bridged measurement is correct. If a 6 dB difference is noted, the terminated measurement is correct.

5.2. POWER

5.2.1. Connect a DC voltmeter to the TP1 and GND test points on the 41620 Power Supply. Turn power ON and read -20.0 VDC. Adjust R15 of the 41620 module, if required.

5.3. VF TRANSMIT LEVEL

5.3.1. Insert a 1 KHz test tone from a signal generator into the TEST TONE jacks at a level of –16 dBm.

5.3.2. Connect an AC voltmeter (bridging) to the XMT jacks. Read the level specified by Attachment A. Adjust R58 (coarse) or R59 (fine) on the 41651 Transmit, if required.

5.4. DATA TRANSMIT LEVEL

5.4.1. Insert a 1 KHz test tone from a signal generator into the EXT XMT IN jacks. Set the signal generator level as specified by Attachment A.

5.4.2. Connect an AC voltmeter (bridging) to the XMT jacks. Read the level specified by Attachment A. Adjust R65 on the 41651 Transmit, if required.

5.5. TRANSMIT SIGNALING LEVEL

5.5.1. Connect an AC voltmeter (bridging) to the XMT jacks.

5.5.2. Go off hook and select digit "1" on the keyboard. Read the level specified by Attachment A. Adjust R8 on the 416-111 Front Motherboard Assembly on the front panel, if required.

5.6. VF RECEIVE LEVEL

5.6.1. Insert a 1 KHz test tone from a signal generator into the RCV jacks. Set the signal generator level as specified by Attachment A.

5.6.2. Connect an AC voltmeter (terminate with 600Ω) to the 4W OUT jacks. Read a level of +7 dBm. Adjust R40 on the 41650 Receive, if required.

5.7. DATA RECEIVE LEVEL

5.7.1. Insert a 1 KHz test tone from a signal generator into the RCV jacks. Set the signal generator level as specified by Attachment A.

5.7.2. Connect an AC voltmeter (terminate if required) to the EXT RCV OUT jacks. Read the level specified by Attachment A. Adjust R43 on the 41650 Receive, if required.

5.8. TWO-CHANNEL INTERFACE LEVELS

5.8.1. Turn power OFF. Remove the 41687 Multi-Channel Interface module and insert an Extender Card into the module position. Insert the 41687 module into the Extender Card. Turn power ON.

5.8.2. Insert a 1 KHz test tone from a signal generator into the TEST TONE jacks at a level of –16 dBm.

5.8.3. Set the channel select push button switches on the front panel such that only Channel 1 is selected. Connect an AC voltmeter (terminate if required) to pins 11 and 12 on the Extender Card. Read the level specified by Attachment A for CH1 XMT. Adjust R75 on the 41687 module, if required.

5.8.4. Set the channel select push button switches on the front panel such that only Channel 2 is selected. Connect the AC voltmeter (terminate if required) to pins 13 and 14 on the Extender Card. The signal generator is still connected to the TEST TONE jacks as in step 5.8.2. Read on the AC voltmeter the level specified by Attachment A for CH2 XMT. Adjust R74 on the 41687, if required.

5.8.5. Connect the signal generator to pins P and R on the Extender Card. Set the signal generator to 1 KHz at the level specified by Attachment A for CH2 RCV. Connect the AC voltmeter (terminated with 600Ω) to the 4W OUT jacks and read a level of +7dBm. Adjust R91 on the 41687 module, if required.

5.8.6. Set the channel select switches on the front panel such that only Channel 1 is selected. Connect the signal generator to pins M and N on the Extender Card. Set the signal generator to 1 KHz at the level specified by Attachment A for CH1 RCV. With the AC voltmeter still connected to the 4W OUT jacks, read a level of +7 dBm. Adjust R92 on the 41687 module, if required.

5.8.7. Turn power OFF. Remove the 41687 module and Extender Card. Replace the 41687 module in its position.

5.9. 4W/4W or 6W/4W BRIDGE LEVELS (if installed)

5.9.1. With power OFF, remove the 41685 Bridge from J2 (AUX Bridge 1) and insert an Extender Card into the module position. Insert the 41685 Bridge into the Extender Card. Turn power ON.

5.9.2. Connect a 1 KHz test tone from a signal generator to pins 21 and 22 (LEG 1 IN) on the Extender Card. Set the level as specified by Attachment A.

5.9.3. Connect an AC voltmeter (terminate if required) to pins F and H (LEG 2 OUT) on the Extender Card. Read the level specified by Attachment A. Adjust R2 on the 41685 module, if required.

5.9.4. Connect an AC voltmeter (terminate if required) to pins K and L (LEG 3 OUT) on the Extender Card. Read the level specified by Attachment A. Adjust R3 on the 41685 module, if required.

5.9.5. Connect an AC voltmeter (terminate if required) to pins M and N (LEG 4 OUT) on the Extender Card. Read the level specified by Attachment A. Adjust R4 on the 41685 module, if required.

NOTE: *Perform steps 5.9.6. and 5.9.7. only if Option -01 is installed on the 41685 module*.

5.9.6. Connect an AC voltmeter (terminate if required) to pins R and S (LEG 5 OUT) on the Extender Card. Read the level specified by Attachment A. Adjust R5 on the 41685-01 module, if required.

5.9.7. Connect an AC voltmeter (terminate if required) to pins T and U (LEG 6 OUT) on the Extender Card. Read the level specified by Attachment A. Adjust R6 on the 41685-01 module, if required.

5.9.8. Connect the signal generator to pins 19 and 20 (LEG 2 IN) on the Extender Card. Set the signal generator level as specified by Attachment A. Read the same level on the AC voltmeter as obtained in the last step performed (step 5.9.5. or step 5.9.7. for option -01). Adjust R8 on the 41685 module, if required.

5.9.9. Connect the AC voltmeter (terminate if required) to pins D and E (LEG 1 OUT) on the Extender Card. Read the level specified by Attachment A. Adjust R1 on the 41685 module, if required.

5.9.10. Connect the signal generator to pins 16 and 17 (LEG 3 IN) on the Extender Card. Set the level as specified by Attachment A. Read the same level on the AC voltmeter as obtained in step 5.9.9. Adjust R9 on the 41685 module, if required.

5.9.11. Connect the signal generator to pins 14 and 15 (LEG 4 IN) on the Extender Card. Set the level as specified by Attachment A. Read the same level on the AC voltmeter as obtained in step 5.9.9. Adjust R10 on the 41685 module, if required.

NOTE: *Perform steps 5.9.12. and 5.9.13. only if Option -01 is installed on the 41685 module*.

5.9.12. Connect the signal generator to pins 11 and 12 (LEG 5 IN) on the Extender Card. Set the level as specified by Attachment A. Read the same level on the AC voltmeter as obtained in step 5.9.9. Adjust R11 on the 41685-01 module, if required.

5.9.13. Connect the signal generator to pins 9 and 10 (LEG 6 IN) on the Extender Card. Set the level as specified by Attachment A. Read the same level on the AC voltmeter as obtained in step 5.9.9. Adjust R12 on the 41685-01 module, if required.

5.9.14. Turn power OFF. Remove the 41685 module and Extender Card from J2. Insert the 41685 module into J2.

5.9.15. Repeat steps 5.9.1. through 5.9.14. for the 41685 module in J3 (AUX BRIDGE 2), if installed.

This concludes the alignment procedure.

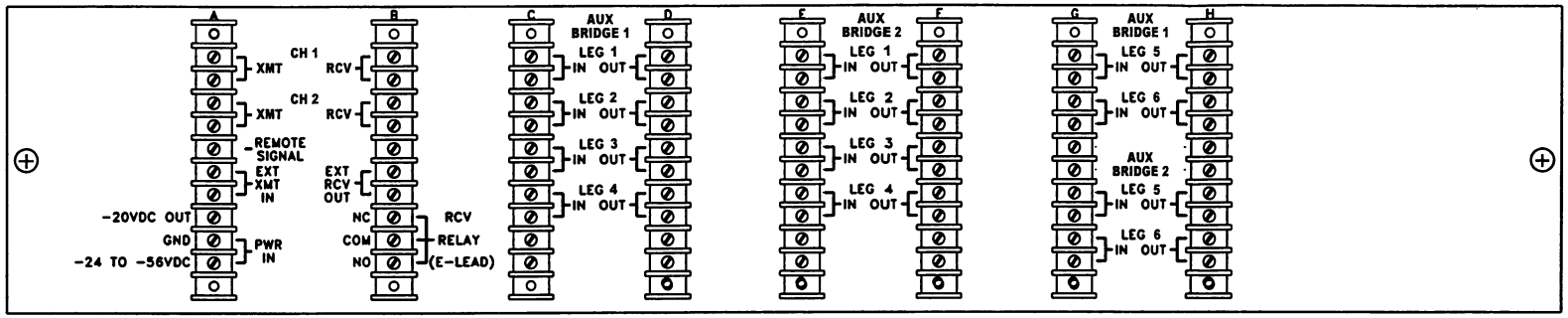


Figure 1 Option 602/285

(2 Ch. Order Wire with two 4 Way or 6 Way Bridges)

REAR PANEL VIEW

SHEET 1

CAD 56022853

03	ECO 1454	DHS			6/98
ISSUE	REVISION				DATE

DRAWN: DHS

CHECKED:

APPROVED:

DATE: 6/23/98

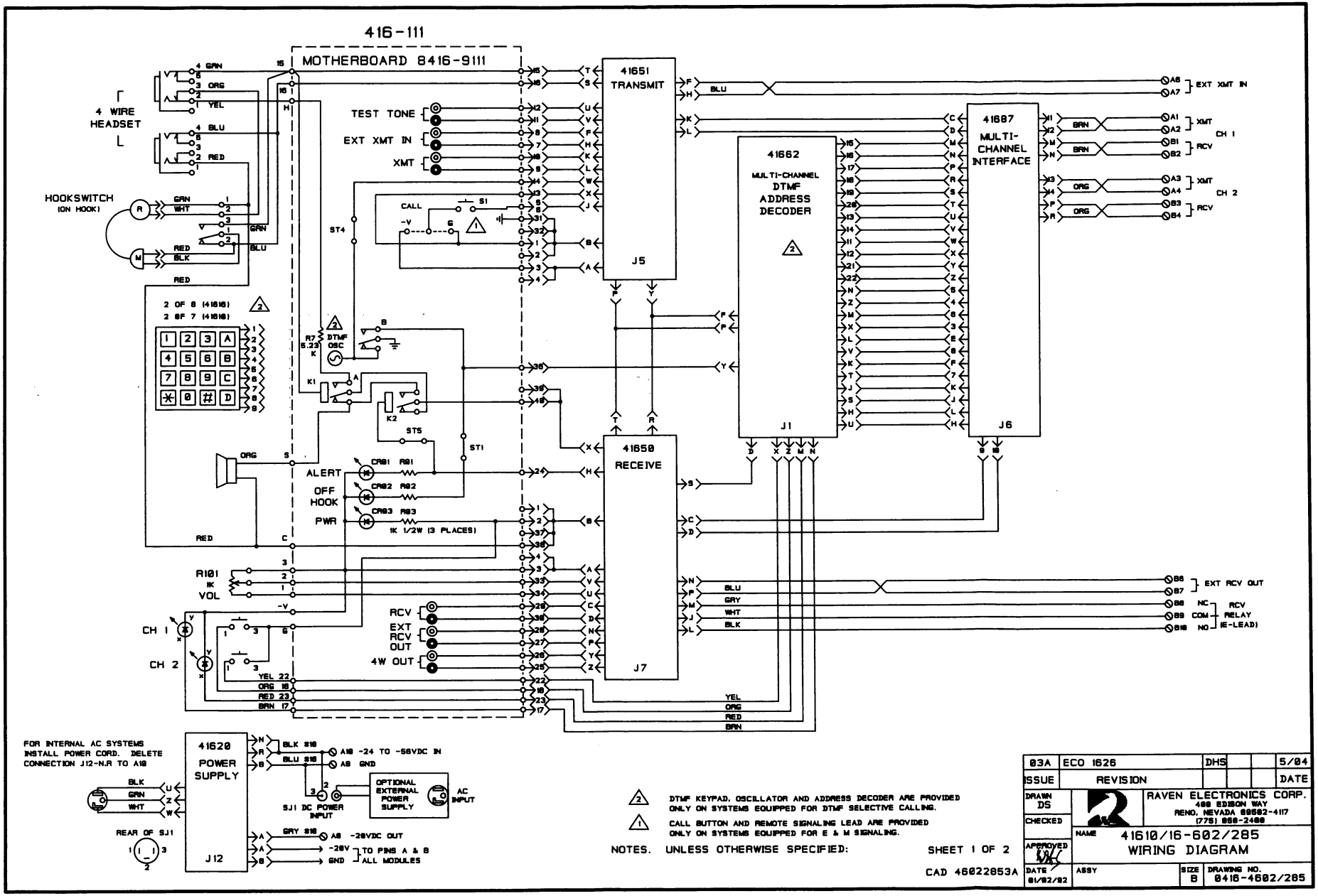
RAVEN ELECTRONICS CORP.
400 EDISON WAY
RENO, NEVADA 89502-4117
(702) 858-2400

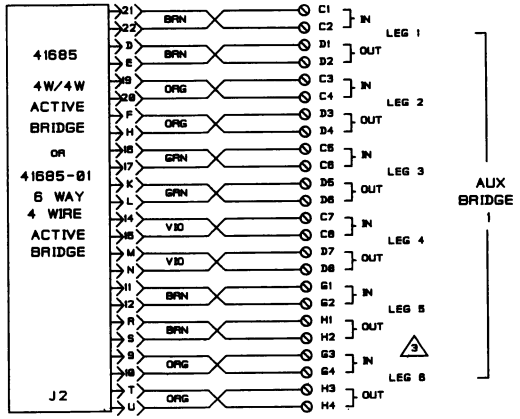
NAME: 41610/16-602/285 CHASSIS ASSEMBLY DRAWING

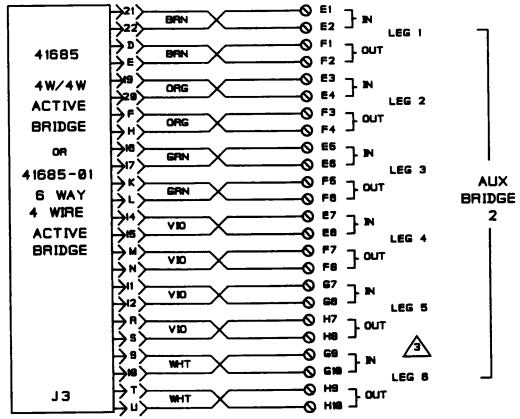
ASSY:

SIZE: B

DRAWING NO: 0416-5602/285


416-111
MOTHERBOARD 8416-9111
4 WIRE HEADSET
HOOKSWITCH (ON HOOK)
2 OF 8 (41618)
2 OF 7 (41618)
TEST TONE
EXT XMT IN
XMT
CALL
S1
ST4
ST5
ST1
K1
K2
R7 5.23K DTMF OSC
ALERT
OFF HOOK
PWR
CR81 R81
CR82 R82
CR83 R83
1K 1/2W (3 PLACES)
R101 1K VOL
CH 1
CH 2
RCV
EXT RCV OUT
4W OUT
41651 TRANSMIT
J5
41650 RECEIVE
J7
41662 MULTI-CHANNEL DTMF ADDRESS DECODER
J1
41687 MULTI-CHANNEL INTERFACE
J6
EXT XMT IN
XMT
CH 1
RCV
CH 2
EXT RCV OUT
RCV RELAY (E-LEAD)
NC
COM
NO
41620 POWER SUPPLY
J12
SJ1 DC POWER INPUT
OPTIONAL EXTERNAL POWER SUPPLY
AC INPUT
REAR OF SJ1
A10 -24 TO -56VDC IN
A9 GND
A8 -28VDC OUT
-28V
GND
TO PINS A & B ALL MODULES
FOR INTERNAL AC SYSTEMS INSTALL POWER CORD. DELETE CONNECTION J12-N,R TO A10
DTMF KEYPAD, OSCILLATOR AND ADDRESS DECODER ARE PROVIDED ONLY ON SYSTEMS EQUIPPED FOR DTMF SELECTIVE CALLING.
CALL BUTTON AND REMOTE SIGNALING LEAD ARE PROVIDED ONLY ON SYSTEMS EQUIPPED FOR E & M SIGNALING.
NOTES. UNLESS OTHERWISE SPECIFIED:
SHEET 1 OF 2
CAD 46022853A
03A ECO 1626 DHS 5/04
ISSUE REVISION DATE
DRAWN DS
CHECKED
APPROVED
DATE 01/02/02
RAVEN ELECTRONICS CORP.
466 EDISON WAY
RENO, NEVADA 89502-4117
(775) 856-2466
NAME 41610/16-602/285
WIRING DIAGRAM
ASSY
SIZE B
DRAWING NO. 8416-4602/285





3 ORDER WIRE IS WIRED FOR BUT NOT NECESSARILY EQUIPPED WITH OPTIONAL 6 WAY BRIDGE

03A	ECO 1626	DHS			5/04
ISSUE	REVISION				DATE

DRAWN DS
CHECKED
APPROVED
DATE 01/02/02

RAVEN ELECTRONICS CORP.
400 EDISON WAY
RENO, NEVADA 89502-4117
(775) 858-2400

NAME 41610/16-602/285
WIRING DIAGRAM

ASSY | SIZE B | DRAWING NO. 0416-4602/285

CAD 46022853A

FUNCTION	REAR TERMINAL CONNECTIONS	SUGGESTED WIRE
POWER	A10 or SJ1 SLEEVE -24 to -56V A9 or SJ1 CENTER Ground or Power Cord for AC System	18 GA.
EXT XMT IN	A6,A7	24 GA.
EXT RCV OUT	B6,B7	24 GA.
CH1 XMT	A1,A2	24 GA.
CH1 RCV	B1,B2	24 GA.
CH2 XMT	A3,A4	24 GA.
CH2 RCV	B3,B4	24 GA.
AUX BRIDGE 1		
LEG 1 IN	C1,C2	24 GA.
LEG 1 OUT	D1,D2	24 GA.
LEG 2 IN	C3,C4	24 GA.
LEG 2 OUT	D3,D4	24 GA.
LEG 3 IN	C5,C6	24 GA.
LEG 3 OUT	D5,D6	24 GA.
LEG 4 IN	C7,C8	24 GA.
LEG 4 OUT	D7,D8	24 GA.
LEG 5 IN	G1,G2	24 GA.
LEG 5 OUT	H1,H2	24 GA.
LEG 6 IN	G3,G4	24 GA.
LEG 6 OUT	H3,H4	24 GA.

FUNCTION	REAR TERMINAL CONNECTIONS	SUGGESTED WIRE
AUX BRIDGE 2		
LEG 1 IN	E1,E2	24 GA.
LEG 1 OUT	F1,F2	24 GA.
LEG 2 IN	E3,E4	24 GA.
LEG 2 OUT	F3,F4	24 GA.
LEG 3 IN	E5,E6	24 GA.
LEG 3 OUT	F5,F6	24 GA.
LEG 4 IN	E7,E8	24 GA.
LEG 4 OUT	F7,F8	24 GA.
LEG 5 IN	G7,G8	24 GA.
LEG 5 OUT	H7,H8	24 GA.
LEG 6 IN	G9,G10	24 GA.
LEG 6 OUT	H9,H10	24 GA.

1. REFERENCES

1416-1202 Regulated Power Supply Schematic

2. GENERAL

The Raven 41620 Regulated Power Supply provides a regulated -20 Volt DC (@ 1.2A max.) output from an unregulated supply.

The 41620 has two input power options available. The 41620-01 regulates an input voltage ranging from -24 to –56 VDC. The 41620-02 provides a regulated output from either a 110 VAC or a 220VAC (50/60Hz) source.

The 41620 provides foldback current limiting at an output current of approximately 1.2 amperes. The 41620 can be modified at the factory to increase the maximum output current if required. Included on the 41620 is an ON/OFF power switch and a fuse in series with the input. The output is factory set at –20 VDC but is adjustable from –18 VDC to –24 VDC.

3. SPECIFICATIONS

Input Voltage	
Option -01	-24 VDC TO –56 VDC
Option -02	110 VAC or 220 VAC (50/60 Hz)
Output Voltage	-20 VDC regulated -18 VDC to –24 VDC adjustment range
Output Current	1 ampere @ -20 VDC foldback current limiting occurs @ approximately 1.2A
Output Voltage Ripple	≤ 75 mv (full load)

4. THEORY OF OPERATION

Power input to the 41620 is derived from either a -24 to –56 VDC source in the 41620-01 version or from a 110VAC or 220VAC 50/60Hz source in the 41620-02 version.

4.1. 41620-01 DC OPTION

The DC input voltage is applied between pins R, S, (optionally pin D or pin N) and Ground (pin B) through CR8, fuse F1, power switch S1 and the "DC" strap. The input voltage is then applied to the emitter of the series pass transistor Q1 via R9.

4.2. 41620-02 AC OPTION

The AC input is applied to pins U and W with the external ground connected to pin Y or Z. The input voltage completes the circuit through "AC" strap, fuse F1 and power switch S1 to the primary of transformer T1. T1 steps down the incoming 110 VAC or 220 VAC to a nominal 32 VAC.

The 32 VAC is full wave rectified by the silicon bridge rectifier CR1. Capacitor C1 helps eliminate the ripple component on the unregulated DC. The unregulated DC is applied to the emitter of the series pass transistor Q1 via R9.

4.3. DC REGULATOR

U1 is a 723 Integrated Circuit voltage regulator which provides a regulated output to the base of transistor Q2. Q2 provides the current drive to the base of the series pass transistor Q1.

Resistors R11 and R12 form a voltage divider that is referenced to the –20 V regulated output and driven by the "Voltage Reference Output" of the 723. This combination provides a voltage that is fixed in reference to the –20 V regulated output. This voltage drives the "Inverting Input" of the 723. The voltage for the "Non-inverting Input" of the 723 is determined by the setting of R15 in combination with R13 and R14. R15 is used to adjust the –20 V regulated output, which can be monitored at TP1. Both R15 and TP1 are near the switch at the front of the board for easy access.

4.4. FOLDBACK CIRCUITRY

R9, R1, R2, and Q4 comprise a current sensing circuit and determine when foldback occurs. R5 and R6 provide a reference voltage to the inverting input of comparator U2.

A –16 VDC supply is derived from the input voltage via R8, CR2, and C3 to power comparator U2. R3, R4, and CR4 provide a secondary reference voltage to the inverting input of comparator U2. These components insure control over the foldback circuitry even when the regulated output voltage drops to 0.

When the output current exceeds 1.2A, transistor Q4 will turn on, causing the output of comparator U2 to switch. This turns transistor Q3 on which turns transistor Q2 off and limits current flow through the series pass transistor Q1. Diode CR5 protects the output of the 723 regulator when foldback occurs.

4.5. CR7 is a "Power On" LED indicator. This LED will be illuminated when the 41620 is turned ON and the regulated output voltage is present.

1. REFERENCES

1416-1501 Receive Schematic

2. GENERAL

2.1. The Raven 41650 Receive module provides wideband (data), voice and speaker outputs from a single balanced input. Amplification is provided on all ports, with a 3-stage low pass filter inserted in the voice and speaker paths. A wide range of input levels can be accepted through the use of level adjustment for all ports. An audible call alert generator is typically included, providing a call indication through the speaker output when enabled. Relay contacts (2 Form C) are available as a simultaneous call indication. The relay is enabled concurrent with audible alert and can be programmed to energize continuously or to cycle on and off with the audible alert.

2.1.1. The -01 option of the 41650 module includes a single frequency signaling detector for use in E&M signaling systems.

2.1.2. The -02 option of the 41650 module makes the output of SF detector (option -01 above) available for off-board use.

2.1.3. The -03 option adds a single-ended voice output.

2.1.4. The -04A option converts the RCV input to a single-ended 75Ω port.

2.1.5. The -04B option converts the RCV input to a single-ended high impedance bridging port (typically 10KΩ).

2.1.6. The -05 option adds capacitors to the feedback loop of both input amplifier stages for high frequency attenuation.

3. SPECIFICATIONS

Power	-20VDC @ 200mA max.
Environmental	
Operating Temperature	0° to 50° C
Relative Humidity	0° to 95% non-condensing
Input/Output Impedance	600Ω balanced, standard
Input Level (RCV)	-46 to +7dBm @ 600Ω
VF Frequency Response	± 1dBm0 500Hz to cutoff frequency, (Ref. @ 1KHz) -3dBm0 @ 300Hz, ≥55dB down @ ¼ octave above cutoff frequency.
Wideband Frequency	± 1dBm0 500Hz to 30KHz, -3dBm0 @ Response (Ref. @ 1KHz) 300Hz, -4dBm0 @ 60KHz.
Harmonic Distortion	<1%
Signaling Frequency (SF)	Customer specified from 1000Hz to 3825Hz
Speaker Output	1W max into 45Ω
Receive Signaling Relay	Dual Form C rated @ 1A @ 125VAC or (E-Lead) 2A @ 30VDC.

4. THEORY OF OPERATION

The 41650 Receive module provides two 600Ω balanced outputs from one RCV input. One output is for VF, and one is the wideband (data) output. A VF speaker amplifier, an alert tone generator E-Lead relay contacts, and when the -01 option is installed, a signal detector are included on the module.

4.1. INPUT AMPLIFIER

The 41650 Receive module has a single 600Ω balanced input which is split into two 600Ω balance outputs as well as a speaker amplifier output. Transformer T1 provides the balanced input as well as excellent common mode rejection and DC isolation. Input amplifier U6A provides the first stage of gain and its output level is adjusted by potentiometer R36. Amplifier U6B is the second stage of gain and its output level is always set to +6dBm nom. (optimum input level into the low pass filter) by potentiometer R40. This output drives the wideband amplifier, the VF path, and, when the -01 Option is installed, the Signaling Detector. Option -05 adds capacitors to the feedback loop of amplifiers U6A and U6B to attenuate their output at frequencies above 16KHz.

4.2. WIDEBAND AMPLIFIER

Amplifier U7A is the wideband amplifier and its output level is adjusted by potentiometer R43. This output drives transformer T2 via impedance matching resistor R41. Transformer T2 provides a balanced output as well as DC isolation for the EXT RCV OUT port.

4.3. VF AMPLIFIER

4.3.1. The signal at the output of amplifier U6B is routed through the low pass filter. The low pass filter used on the 41650 Receive module is a 3 D-element active filter which provides a response of +1, -3dB over a frequency range of 300Hz to the cutoff frequency (Fc, customer specified), and attenuation of ³55dB of signals one quarter octave above Fc. The low pass filter consists of Operational Amplifiers U1, U2, U3 and associated circuitry.

4.3.2. The output of the low pass filter is routed to the input of amplifier U8A. The path from the low pass filter to U8A is strappable such that with ST-9 removed and ST-E1 & ST-F1 installed, the signal can be routed through other modules via pin F, & return via pin E into U8A. U8A is a fixed gain amplifier & drives the 4W OUT via impedance matching resistor R58 & transformer T3, as well as the speaker amplifier.

4.3.3. Option -03 provides a single-ended input (if ST-11 is installed), or single-ended output (if ST-10 is installed) on pin K via resistors R59 and R74 from amplifier U8A. The values of R59 and R74 are factory selected according to the application.

4.4. SPEAKER AMPLIFIER

The speaker amplifier consists of U8B, Q5, Q2, Q3, Q4 and associated circuitry. Inputs from the VF path, the sidetone input (from the 41651 Transmit module), and the alert tone generator are summed into the speaker amplifier. An off-board potentiometer (typically a 1KW 1W potentiometer on the front panel of the Order Wire) connected to pins U and V acts as a shunt to provide a volume control for the VF and sidetone signals. The volume of the alert tone is not affected by the volume control. The speaker amplifier has a maximum output of 1W into a 45Ω speaker with <2% harmonic distortion.

4.5. ALERT TONE GENERATOR

4.5.1. The Alert Tone Generator is an option that is more commonly installed than not. It is deleted in cases where another source for the alert tone is more desirable.

4.5.2. Two alert tone frequencies are available & are selected via 3 programming jumpers. When the jumpers are in the "LO" position, the frequency is 360Hz. When the jumpers are in the "HI" position, the frequency is 1940Hz. Potentiometer R72 can be used to adjust the alert tone volume(1 watt max. to .1 watt min.).

4.5.3. The Alert Tone Generator consists of U11, U9, and associated components. U11 is a free running oscillator which generates the alert tone (360Hz or 1940Hz) as well as the output to gate the tone ON and OFF at preset rates through U9. The outputs of U9 are coupled to the speaker amplifier. The ALERT tone is activated by grounding pin R. The ALL CALL tone is activated by grounding pin S (ST-4 installed). The ALL CALL tone is gated at approximately .5 secs. OFF and .5 secs. ON, while the ALERT tone is gated at approximately 1.5 secs. OFF and 1.5 secs. ON.

4.5.4. Activating either the ALERT or ALL CALL energizes relay K1. This two form C relay provides an E-Lead indication as well as driving the ALERT indicator on the Order Wire front panel (when provided). Two modes of operation can be selected, 1) the relay is continuously energized for the duration of the alert tone (CO position of the programming jumper), or 2) the relay will cycle on and off at the same rate as the alert tone (CY position of the programming jumper).

4.6. SIGNALING DETECTOR

When the -01 option is installed, a signaling detector is included as a part of the 41650 module. The signaling detector consists of a narrow band pass filter (U5A, U4A, U4B, and associated circuitry), a peak detector (D1, R29, R30, C14, C15), and a comparator (U5B). Potentiometer R25 adjusts the overall gain and potentiometer R24 adjusts the center frequency of the filter. When the voltage across C15 exceeds the comparator reference voltage (pin 6 of U5B), the comparator output switches high activating the alert tone generator (U11,U9) and the receive relay K1 via transistor Q1.

4.7. Option -02 pins out the signal detector output (pin 7 of comparator U5B) on pin W. If strap ST-5 is installed, the output is routed directly from comparator U5B and is active high (GND). If ST-5 is deleted and transistor Q6 and its associated resistors are installed, Q6 inverts the output of U5B, making the output at pin W active low (-20VDC).

4.8. Option -03 provides a single-ended voice input or single-ended voice output when R59, R74, and C36 are installed. The value of each component is determined by the application. A typical use for the input is to sum an auxiliary tone or voice path into the speaker amp. A typical use for the output is to drive the earpiece from a remotely located headset or telephone.

4.9. Option -04 changes the configuration of the input amplifier for a single-ended 75Ω input (terminating or bridging). Transformer T1 is deleted and a .33μf ceramic capacitor is installed in its place for DC isolation. Pin C of the 41650 module is the signal input, and pin D is ground. For a 75Ω terminating input, a 75Ω resistor is installed across pins C and D. For a high impedance bridging input, the 75Ω resistor is deleted.

4.10. Option -06 adds capacitance to the feedback loop of both stages of the input amplifier, U6A and U6B. The capacitance value is selected to attenuate frequencies above the spectrum utilized by the wideband (data) port.

1. REFERENCES

1416-1511 Transmit Schematic

2. GENERAL

2.1. The Raven 41651 Transmit Module provides a single balanced output from multiple VF inputs, a wideband (data) input, and a signaling oscillator. Amplification is provided on all ports, with a 3-stage low pass filter inserted in the voice path. All ports have potentiometer level adjustment and can accommodate a wide range of output levels.

2.1.1. The -01 Option of the 41651 Module includes a single frequency signaling oscillator for use in E&M signaling systems.

2.1.2. The -02 Option of the 41651 Module includes a ringback tone oscillator for call acknowledgment (typically used only in DTMF selective signaling systems).

2.1.3. The -03A Option converts the XMT output to a single-ended 75Ω port.

2.1.4. The -03B Option converts the XMT output to a single-ended high impedance bridging port.

2.1.5. The -04 Option supplies talk battery for a remote MIC at pins M and N (4-wire input).

2.1.6. The -05 Option XMT relay will prevent any transmission at pins K and L until the transmit path is enabled at pin Y (typically DTMF correct address) or at pin Z (typically off hook condition).

3. SPECIFICATIONS

Power	-20VDC @ 50mA max
Environmental	
Operating Temperature	0°C to 50°C
Relative Humidity	0% to 95% non-condensing
Input/Output Impedance	600Ω balanced, standard
Output Level (XMT)	+7 dBm max. -46 dBm min. @ 600Ω
Idle Noise (XMT)	<10 dBrnC0
VF Frequency Response	±1 dBm0 500 Hz to cutoff frequency
(Ref. @ 1KHz)	-3 dBm0 @ 300 Hz
	≥55 dB down @ ¼ octave above cutoff frequency
Wideband Frequency Response	±1 dBm0 500Hz to 30KHz
(Ref. @ 1KHz)	-3dBm0 @ 300Hz, -4dBm @ 60KHz
Harmonic Distortion	<1%
Signaling Frequency (SF)	Customer specified from 1000 Hz to 3825 Hz

4. THEORY OF OPERATION

The 41651 Transmit Module has five 600Ω balanced inputs which are summed into one output. Four of these inputs are for VF and one is the wideband (data) input. In addition, the -01 Option signaling oscillator, and the -02 Option ringback oscillator are summed into the wideband path. Output amplifier U7B combines the VF and wideband paths and drives the output transformer T1 via impedance matching resistor R61.

4.1. VF AMPLIFIER

4.1.1. VF signals enter the module at the DTMF input (pins W and X), the 4-wire input (pins M and N), the TEST TONE input (pins U and V), and the MIC input (pins S and T) which also provides talk battery to the microphone. These inputs are all balanced with 600Ω impedance. Unused inputs need no external termination.

4.1.2. All VF signals are summed at pins 2 and 6 of the differential summing amplifier, U6. The signal at the output of U6B (pin 7) is coupled to the low pass filter and also to pin P which provides local sidetone. The path from U6B to the low pass filter is strappable such that with the strap removed, the signal can be routed through other modules via pin P, and return via pin R into the low pass filter.

4.1.3. The low pass filter used in the 41651 Transmit is a 3 D-element active filter which provides a response of +1, -3 dB over a frequency range of 300Hz to the cutoff frequency (Fc, customer specified), and attenuation of ≥55 dB of signals one quarter octave or more above Fc. The low pass filter consists of operational amplifiers U1, U2, U3 and associated circuitry. The output of the low pass filter is routed to the input of amplifier U7B via potentiometer R58.

4.2. WIDEBAND AMPLIFIER

Wideband signals enter the 41651 Transmit Module on pins F and H and are routed to transformer T2 which provides a balanced input as well as excellent common mode rejection and DC isolation. U7A is the wideband amplifier and potentiometer R65 adjusts the level of the wideband path.

4.3. OUTPUT AMPLIFIER

Amplifier U7B is a single stage amplifier which provides a maximum output of +7dBm into a 600Ω load at pins K and L. The gain of U7B is fixed at one of two levels, selected by a programming jumper. The "LG" jumper (ST6) sets the gain at 0 dB and should be used when the output level of the 41651 Module is -10 dBm (@ 600Ω) or less. The normal gain of U7B is +15 dB which is used when the output level of the 41651 Module is greater than -10 dBm (@ 600Ω), or when Option -03A or Option -03B is installed.

4.4. SIGNALING OSCILLATOR

When the -01 Option is installed, a signaling oscillator is included as a part of the 41651 Module. The signaling oscillator consists of U4, U5 and associated circuitry. The oscillator can be enabled by applying the appropriate voltage to pin D (if ST1 is installed) or pin J. If -01A is installed, -20VDC applied to pins D or J will enable the oscillator, or if -01B is installed, ground on pins D or J will enable the oscillator. The frequency of the signal oscillator is adjusted by R24. The output of the oscillator is coupled through C15 to R35. R35 is the coarse adjustment of the level of the oscillator, and R36 is the fine level adjustment. The oscillator signal then goes to pin 6 of output amplifier U7B and is summed into the transmit output.

4.5. RINGBACK OSCILLATOR

The -02 Option provides ringback tones for call acknowledgment. Oscillator/counter U8 digitally generates the required frequencies when enabled by a ground at pin Y. U9 gates the frequencies to create a ringback tone. The signal then goes to U7B and thus to the transmit output.

4.6. SINGLE ENDED OUTPUT

The -03 Option converts the output amplifier for a single-ended 75Ω output (terminating or bridging). Transformer T1 and resistor R61 are deleted and a .33μf ceramic capacitor and a 3.3KΩ resistor are installed. For Option -03A, a 75Ω 1% resistor is included to terminate the port. For Option -03B, the 75Ω resistor is deleted for high impedance (typically 3.3KΩ) bridging port.

4.7. TALK BATTERY

The -04 Option provides talk battery for the use of a remote handset or headset microphone.

4.8. TRANSMIT RELAY

The -05 Option, relay K1, isolates the circuitry on the 41651 Module from the transmit port to minimize idle noise. The relay is energized and connects the transmit path when an off hook condition exists, or when ringback is being transmitted.

1. REFERENCES

1416-1620 Multi-Channel DTMF Address Decoder Schematic

2. GENERAL

The Raven 41662 Multi-Channel DTMF Address Decoder provides 2 of 7 and 2 of 8 DTMF tone detection and call decoding for two (2), three (3) (Option -02), or six (6) (Option -01) channels using one, two, or three digit addressing schemes. Call decoding is performed by setting binary switches (up to three per correct address) to respond to the desired DTMF digits. Two Correct Address outputs are available. The Correct Address outputs can be reset either by external resets corresponding to the Correct Address, or a programmable time out. The DTMF "ALL CALL" and "ALL CLEAR" tone pairs have outputs provided. Outputs are provided for ringback and for local call indicators. The inputs to the DTMF receivers are balanced high impedance inputs, to prevent loading of the receive lines.

3. SPECIFICATIONS

Power	-20VDC @ 140 mA max.
Environmental	
Operating Temperature	0° to 50°C
Relative Humidity	0 to 95%
Input	
Impedance	100KΩ @ 1KHz
DTMF Detect Level	-35 to –5 dBm with ST1-4, 9, 10 in LO position -21 to +9 dBm with ST1-4, 9, 10 in HI position
DTMF Tones	
Detector Bandwidths	± 2.5%
Allowable Twist	± 12dB
Minimum Tone Duration	40mSec
Minimum Inter-Digit pause	40mSec
Inter-digit Time-out	
Maximum Time	5 seconds
Outputs	
ALL CALL, ALL CLEAR, Correct Address 1, and Correct Address 2.	Open Collector, Ground when active
Ringback 1 through 6	20mA to Ground when active

4. ADDRESS DIGIT PROGRAMMING

The 41662 Multi-Channel DTMF Address Decoder detects Dual Tone Multi-Frequency (DTMF) signals to provide selective address decoding functions. DTMF signals are unique tone pairs generated by standard Touch Tone encoder arrays. Each button on a Touch Tone encoder is identified by the pair of frequencies generated when the button is pushed. Four low- group frequencies correspond to the four rows of buttons and four high-group frequencies correspond to the four columns. The fourth column (1633Hz) is typically used only in special control applications.

To program the 41662 Multi-Channel DTMF Address Decoder, determine the number of digits to be used (one, two, or three) for Correct Address 1 (and Correct Address 2, if used), and set the appropriate binary encoded switches. Three binary encoded switches labeled S1, S2, and S3 are programming switches for the first, second, and third digits, respectively, for Correct Address 1. Three binary encoded switches labeled S4, S5, and S6 are programming switches for the first, second, and third digits, respectively, for Correct Address 2. Each number on the binary encoded switch corresponds to a DTMF digit, as shown in Table I. The DTMF digit "ALL CLEAR" (#) cannot be programmed as part of the correct address, as receiving an "ALL CLEAR" will clear down all received DTMF digits for that particular channel. The DTMF digit "ALL CALL" can be programmed as part of the correct address. Letter "F" on the switches is decoded as a non- digit. When a non-digit is decoded, any switch setting after the non-digit will be ignored, i.e. if the 2nd digit switch is set to "F", digits two and three will be ignored (one digit correct address).

If Correct Address 1 or Correct Address 2 is not used, setting S1 or S4, respectively, to "F" will provide this function.

EXAMPLE:

If Correct Address 1 is 456, S1 is set to 4, S2 is set to 5, and S3 is set to 6. If Correct Address 2 is 19, S4 is set to 1, S5 is set to 9, and S6 is set to "F".

TABLE I

PROGRAMMING FOR S1 THROUGH S6	
SWITCH POSITION	DTMF DIGIT
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
A	A
B	B
C	C
D	D
E	ALL CALL
F	NON DIGIT

5. CORRECT ADDRESS RING TIME PROGRAMMING

5.1. S7 programs the correct address time-out. Switch positions 0 through 9 represent 5-second increments, and switch positions "A" through "F" represent 10-second increments. To program the correct address time-out, determine the desired time-out and set S7 as shown in Table II.

TABLE II

PROGRAMMING FOR S7	
SWITCH POSITION	TIME OUT PERIOD
0	5 SEC.
1	10 SEC.
2	15 SEC.
3	20 SEC.
4	25 SEC.
5	30 SEC.
6	35 SEC.
7	40 SEC.
8	45 SEC.
9	50 SEC.
A	60 SEC.
B	70 SEC.
C	80 SEC.
D	90 SEC.
E	100 SEC.
F	110 SEC.

6. STRAP PROGRAMMING

6.1. ST-5 controls the Correct Address 1 (CA1) output (pin F). When ST-5 is not installed, CA1 is reset by (1) another DTMF digit (ALL CLEAR included), (2) a Correct Address 1 timeout, or (3) a reset (active high) on RESET 1 (pin Y) AND a reset (active high) on the Channel Reset that generated the Correct Address 1. When ST-5 is installed, CA1 is reset only by a reset on RESET 1 AND a reset on the Channel Reset that generated the Correct Address 1. Installing ST-5 also controls the RB outputs associated with Correct Address 1, i.e. no more time-out. The RB output will stay active until the CA1 output is reset.

6.2. ST-6 controls the Correct Address 2 (CA2) output (pin E). When ST-6 is not installed, CA2 is reset by (1) another DTMF digit (ALL CLEAR included), (2) a Correct Address 2 time-out, or (3) a reset (active high) on RESET 2 (pin W) AND a reset (active high) on the Channel Reset that generated the Correct Address 2. When ST-6 is installed, CA2 is reset only by a reset on RESET 2 AND a reset on the Channel Reset that generated the Correct Address 2. Installing ST-6 also controls the RB outputs associated with Correct Address 2, i.e. no more time-out. The RB output will stay active until the CA2 output is reset.

6.3. ST-7 controls the RB outputs. When ST-7 is not installed, the RB outputs produce a ringback signal when active. When ST-7 is installed the RB outputs provide a DC level.

6.4. ST-8 is used in conjunction with ST-5 and/or ST-6. When ST-8 is not installed, resetting CA1 or CA2 is controlled as described in 6.1. and 6.2. When ST-8 is installed, CA1 and CA2 can be reset also by a DTMF ALL CLEAR (#).

7. THEORY OF OPERATION

7.1. POWER UP INITIALIZATION

When power is applied, the Z-8 Microcomputer Unit (MCU) (U-1) initializes its ports to the off state and enables a 2.5mSec and a 25mSec clock. The MCU then reads the correct address switches and the correct address timer switch and initializes its internal registers. All internal channel registers are reset to the all clear status.

7.2. DTMF TONE DETECTORS

7.2.1. DTMF input signals are received at the op-amps U-8 and U-9. The op-amps convert the balanced input to a single ended output for the DTMF receivers U-10 through U-15. Op-amp U-8A provides the bias voltage for the input amplifiers.

7.2.1.1. DTMF signals from Channel 1 connect to Input #1 (pins 15 and 16). Signals are routed to the input of op-amp U-9D. The output of the op-amp connects to the DTMF receiver (U-15).

7.2.1.2. DTMF signals from Channel 2 connect to Input #2 (pins 17 and 18). Signals are routed to the input of op-amp U-9C. The output of the op-amp connects to the DTMF receiver (U-14).

7.2.1.3. DTMF signals from Channel 3 connect to Input #3 (pins 19 and 20). Signals are routed to the input of op-amp U-9B. The output of the op-amp connects to the DTMF receiver (U-13) (Option -01 or Option -02).

7.2.1.4. DTMF signals from Channel 4 connect to Input #4 (pins 13 and 14). Signals are routed to the input of op-amp U-9A. The output of the op-amp connects to the DTMF receiver (U-12) (Option -01).

7.2.1.5. DTMF signals from Channel 5 connect to Input #5 (pins 11 and 12). Signals are routed to the input of op-amp U-8D. The output of the op-amp connects to the DTMF receiver (U-11) (Option -01).

7.2.1.6. DTMF signals from Channel 6 connect to Input #6 (pins 21 and 22). Signals are routed to the input of op-amp U-8C. The output of the op-amp connects to the DTMF receiver (U-10) (Option -01).

7.2.2. The DTMF receivers combine switched-capacitor and digital frequency measuring techniques to decode the DTMF signals to four-bit binary data. When a tone is received, the DTMF receiver brings its strobe (pin 15) active.

7.3. CORRECT ADDRESS DETECTION

Binary encoded switches S1, S2, and S3 are used to select the digits to be recognized as Correct Address 1. Binary encoded switches S4, S5, and S6 are used to select the digits to be recognized as Correct Address 2. The positions on the switches correspond to the DTMF digits. To select a digit, set the corresponding switch to the appropriate setting. Refer to section 4 of this description for specific information on address programming.

The MPU starts its scan at Channel 1, and sequentially reads through Channel 6. After Channel 6 has been read, the MPU then tests the Reset lines for each channel. The scan then starts over at channel 1.

When a tone is received, the corresponding DTMF decoder brings its strobe active. The MPU detects the strobe via an 8 to 1 decoder (U-17) and enables the DTMF decoder output via a 1 of 16 selector (U-16). The MPU then reads the DTMF data and compares it to the correct address switch settings.

If the DTMF digit received is the correct digit for either Correct Address 1 or Correct Address 2, a 5-second inter-digit pause timer is enabled. If the received digit is a wrong digit for Correct Address 1, the internal registers for the corresponding channel are reset. If the received digit is a wrong digit for Correct Address 2, the internal registers for the corresponding channel are reset. If the digit is wrong for both Correct Addresses, all subsequent digits will be ignored except for ALL CALL (7.4) and ALL CLEAR (7.5). This allows dialing to proceed without alerting the Order Wire. After dialing ceases for 5 seconds, DTMF decoding will resume.

If the DTMF digit received completes the correct address for Correct Address 1 or Correct Address 2, the corresponding Correct Address output (pin F or E, respectively) is brought active if RESET 1 or RESET 2 is off (low). Internal registers for the channel are reset for the corresponding correct address and the correct address time-out timer (set by S-7) is enabled. The ringback output (RINGBACK

ALERT 1, pin N; RINGBACK ALERT 2, pin M; RINGBACK ALERT 3, pin L; RINGBACK ALERT 4, pin K; RINGBACK ALERT 5, pin J; and RINGBACK ALERT 6, pin H) for the channel which enabled the Correct Address, is brought active.

If RESET 1 is active (high) a ringback sidetone is produced at the RINGBACK OUTPUT (pin P).

7.4. ALL CALL

The "ALL CALL" (*) tone pair is provided with a transistor (Q-8) open collector to ground output (pin D). When an "ALL CALL" is detected, output transistor Q-8 and the channel RB output are enabled for the duration of the tone pair. The MPU will logically "OR" "ALL CALL" tone pairs that are received. Thus if Channel 1 and Channel 2 receive the "ALL CALL" tone pair, the "ALL CALL", Channel 1 ringback, and Channel 2 ringback outputs will be active. When the "ALL CALL" on Channel 1 ceases, the Channel 1 ringback output will turn off, and the "ALL CALL" output will stay active. When the "ALL CALL" on Channel 2 ceases, the "ALL CALL" and Channel 2 ringback outputs will go off.

7.5. ALL CLEAR

The "ALL CLEAR" (#) tone pair is provided with a transistor (Q-7) open collector to ground output (pin C). The "ALL CLEAR" operates the same manner as the "ALL CALL" except that the Channel ringback outputs are not enabled.

1. REFERENCES

1416-1850 4-Way or 6-Way/4-Wire Active Bridge Schematic

2. GENERAL

2.1. The Raven 41685 4-Way or 6-Way/4-Wire Active Bridge provides a multipath interface between 4 ports (or 6 ports with Option -01 installed) on a 4-wire basis. An input at one of the ports is routed through to the output of all other ports, with a minimum of interchannel crosstalk. All inputs and outputs are transformer coupled and are balanced. Potentiometer adjustments on all inputs and outputs allow input level coordination and through path gain adjustments.

3. SPECIFICATIONS

Power Input	-20VDC @ 75mA maximum
Environmental	
Operating Temperature	0° to 50° C
Storage Temperature	-40° to +85° C
Relative Humidity	0 to 95% non-condensing
Inputs	
Input Impedance	600Ω balanced
Input Level	-40 to +7dBm
Outputs	
Output Impedance	600Ω balanced
Output Level	-40 to +7dBm continuously adjustable
Through Path Adjustment, Max	±25dB
Interchannel Crosstalk	<-50dB @ 1KHz and unity gain

4. THEORY OF OPERATION

4.1. INPUT CIRCUITRY

4.1.1. Each of the four inputs (six if Option -01 is installed) consists of an input transformer, impedance matching resistor, and an amplifier.

4.1.2. For INPUT LEG 1, R19 is used for impedance matching of the input transformer T7. The input amplifier for INPUT LEG 1 consists of U-2A, R31, R25, and potentiometer R7.

4.1.3. Signals present at INPUT LEG 1 (pins 21 and 22) are coupled through input transformer T7. The signal is then passed through R31, to the input of amplifier U-2A. R25 and potentiometer R7 provide a gain adjustment of -14 to +19dB for amplifier U-2A, and presents the signal at pin 1 of U-2A.

4.1.4. All other inputs have circuitry identical to INPUT LEG 1 and operate the same.

4.1.5. For INPUT LEG 2, R20 is used for impedance matching of the input transformer T8. The input amplifier for INPUT LEG 2 consists of U-2B, R26, R32, and potentiometer R8.

4.1.6. For INPUT LEG 3, R21 is used for impedance matching of the input transformer T9. The input amplifier for INPUT LEG 3 consists of U-4A, R33, R27, and potentiometer R9.

4.1.7. For INPUT LEG 4, R22 is used for impedance matching of the input transformer T10. The input amplifier for INPUT LEG 4 consists of U-4B, R28, R34, and potentiometer R10.

4.1.8. For INPUT LEG 5 (if Option -01 is installed), R23 is used for impedance matching of the input transformer T11. The input amplifier for INPUT LEG 5 consists of U-6A, R35, R29, and potentiometer R11.

4.1.9. For INPUT LEG 6 (if Option -01 is installed), R24 is used for impedance matching of the input transformer T12. The input amplifier for INPUT LEG 6 consists of U-6B, R30, R36, and potentiometer R12.

4.2. OUTPUT AMPLIFIERS

4.2.1. Each LEG output is driven by a 3-input (or 5-input if Option -01 is installed) summing amplifier. The output of the summing amplifier is transformer coupled to provide a balanced output.

4.2.2. The output amplifier for OUTPUT LEG 1 consists of R43, R49, potentiometer R1, U-1A, and transformer T1. R43 provides impedance matching. Resistor Network RN1 sums the inputs from LEGs 2, 3, 4, 5, and 6, (LEGs 5 and 6 are installed for Option -01 only).

4.2.3. Signals present at the summing network (RN1) of OUTPUT LEG 1 are summed and presented to the output amplifier, U-1A. Potentiometer R1 and resistor R49 provide a gain adjustment of -13 to +19dB. The signal is presented at pin 1 of U-1A and routed to output transformer T1. The signal is coupled through to OUTPUT LEG 1 (pins D and E).

4.2.4. All other outputs have identical circuitry as OUTPUT LEG 1, and operate the same.

4.2.5. The output amplifier for OUTPUT LEG 2 consists of R44, R50, potentiometer R2, U-1B, and transformer T2. R44 provides impedance matching. Resistor Network RN2 sums the inputs from LEGs 1, 3, 4, 5, and 6.

4.2.6. The output amplifier for OUTPUT LEG 3 consists of R45, R51, potentiometer R3, U-3A, and transformer T3. R45 provides impedance matching. Resistor Network RN3 sums the inputs from LEGs 1, 2, 4, 5, and 6.

4.2.7. The output amplifier for OUTPUT LEG 4 consists of R46, R52, potentiometer R4, U-3B, and transformer T4. R46 provides impedance matching. Resistor Network RN4 sums the inputs from LEGs 1, 2, 3, 5, and 6.

4.2.8. The output amplifier for OUTPUT LEG 5 (when Option -01 is installed) consists of R47, R53, potentiometer R5, U-5A, and transformer T5. R47 provides impedance matching. Resistor Network RN5 sums the inputs from LEGs 1, 2, 3, 4, and 6.

4.2.9. The output amplifier for OUTPUT LEG 6 (when Option -01 is installed) consists of R48, R54, potentiometer R6, U-5B, and transformer T6. R48 provides impedance matching. Resistor Network RN6 sums the inputs from LEGs 1, 2, 3, 4, and 5.

4.3. VOLTAGE REGULATION

4.3.1. U7-B provides regulation for the -10VDC bias voltage. U7-A, CR1, CR2, R57, R58, Q1, Q2, R55, and R56 provide a -10VDC signal ground for the output transformers.

1. REFERENCES

1416-1870 Six-Channel Interface Schematic

2. GENERAL

The Raven 41687 Six-Channel Interface provides a selective path interface for a maximum of six 4-wire ports. An input signal at the O.W. XMT INPUT is selectively routed to the CHANNEL XMT outputs. Signals present at the CHANNEL RCV inputs are selectively routed to the summing amp and are available at the O.W. RCV OUTPUT. Potentiometer adjustments on the channel inputs and outputs allow input and output level coordination. A standard loading of the module provides a multipath interface for two 4-wire ports, while Option -01 provides that for six 4-wire ports and Option -02 provides that for three 4-wire ports.

3. SPECIFICATIONS

Power Input	-20VDC @ 75ma max.
Environmental	
Operating Temperature	0° to 50°C
Relative Humidity	0 to 95%
Inputs	
Inputs Impedance	600Ω balanced
Input Level, CH. 1-6 RCV's	-16dBm to +7dBm
Input Level, O.W. XMT Input	0dBm, nominal
Outputs	
Output Impedance	600Ω balanced
Output Level, CH. 1-6 XMT's	-16dBm to +7dBm
Output Level, O.W. RCV Output	0dBm, nominal
Interchannel Crosstalk	< -65dB @ unity gain
Return Loss	> 70dB
Frequency Response	300Hz to 20KHz +1 -3dB

4. THEORY OF OPERATION

4.1. VOLTAGE REGULATION

4.1.1. U-12 provides the regulated -15VDC to power the op-amps and transmission gates. The output of U-11A is used to bias the op-amps. U-11B is used as signal ground.

4.2. O.W. XMT INPUT CIRCUITRY

4.2.1. For the O.W. XMT INPUT (pins C and D), R113 terminates the input. The input splitting amplifier consists of C26, C27, R95 through R98, and op-amp U10A . The output of the splitting amplifier connects to transmission gates U9-B, U9-A, U6-B, U6-A, U3-B, and U3-A.

4.2.2. When the CH 1 SEL. (pin 4) is at -15VDC, Channel 1 and transmission gate U9-B are 4-wire.

4.2.3. When the CH 1 SEL. is at GND, Channel 1 and transmission gate U9-B are on. Signals present at the O.W. XMT INPUT are passed through U9-B to the output amplifier. The output amplifier consists of R86 through R88, U7-B, R78, and R75. Potentiometer R75 provides a level adjustment range of +7 to -16dBm (with a nominal level of 0dBm at the O.W. XMT INPUT). The signal from the output amplifier goes to T6 which connects to the CH 1 XMT (pins 11 and 12) port.

4.2.4. The CH 1 RINGBACK SIGNAL IN (pin 5) input consists of C34, C35, C41, R89, and R90. Signals present at this input are summed into the CH 1 XMT output.

4.2.5. When the CH 2 SEL. (pin 3) is at -15VDC, Channel 2 and transmission gate U9-A are OFF.

4.2.6. When the CH 2 SEL. is at GND, Channel 2 and transmission gate U9-A are ON. Signals present at the O.W. XMT INPUT are passed through U9-A to the output amplifier. The output amplifier consists of R65 through R67, U7-A, R77, and R74. Potentiometer R74 provides a level adjustment range of +7 to -16dBm (with a nominal level of 0dBm at the O.W. XMT INPUT). The signal from the output amplifier goes to T5 which connects to the CH 2 XMT (pins 13 and 14) port.

4.2.7. The CH 2 RINGBACK SIGNAL IN (pin 6) input consists of C15, C16, C40, R63, and R64. Signals present at this input are summed into the CH 2 XMT output.

4.2.8. When the CH 3 SEL. (pin 8) is at -15VDC, Channel 3 and transmission gate U6-B are OFF.

4.2.9. When the CH 3 SEL. is at GND, Channel 3 and transmission gate U6-B are ON. Signals present at the O.W. XMT INPUT are passed through U6-B to the output amplifier. The output amplifier consists of R56 through R58, U4-B, R48, and R45. Potentiometer R45 provides a level adjustment range of +7 to -16dBm (with a nominal level of 0dBm at the O.W. XMT INPUT). The signal from the output amplifier goes to T4 which connects to the CH 3 XMT (pins 15 and 16) port.

4.2.10. The CH 3 RINGBACK SIGNAL IN (pin E) input consists of C32, C33, C39, R59, and R60. Signals present at this input are summed into the CH 3 XMT output.

4.2.11. When the CH 4 SEL. (pin 7) is at -15VDC, Channel 4 and transmission gate U6-A are OFF.

4.2.12. When the CH 4 SEL. is at GND, Channel 4 and transmission gate U6-A are on. Signals present at the O.W. XMT INPUT are passed through U6-A to the output amplifier. The output amplifier consists of R35 through R37, U4-A, R47, and R44. Potentiometer R44 provides a level adjustment range of +7 to -16dBm (with a nominal level of 0dBm at the O.W. XMT INPUT). The signal from the output amplifier goes to T3 which connects to the CH 4 XMT (pins 17 and 18) port.

4.2.13. The CH 4 RINGBACK SIGNAL IN (pin F) input consists of C8, C9, C38, R33, and R34. Signals present at this input are summed into the CH 4 XMT output.

4.2.14. When the CH 5 SEL. (pin J) is at -15VDC, Channel 5 and transmission gate U3-B are OFF.

4.2.15. When the CH 5 SEL. is at GND, Channel 5 and transmission gate U3-B are on. Signals present at the O.W. XMT INPUT are passed through U3-B to the output amplifier. The output amplifier consists of R24 through R26, U1-B, R16, and R13. Potentiometer R13 provides a level adjustment range of +7 to -16dBm (with a nominal level of 0dBm at the O.W XMT INPUT). The signal from the output amplifier goes to T2 which connects to the CH 5 XMT (pins 19 and 20) port.

4.2.16. The CH 5 RINGBACK SIGNAL IN (pin K) input consists of C30, C31, C37, R27, and R28. Signals present at this input are summed into the CH 5 XMT output.

4.2.17. When the CH 6 SEL. (pin H) is at -15VDC, Channel 6 and transmission gate U3-A are OFF.

4.2.18. When the CH 6 SEL. is at GND, Channel 6 and transmission gate U3-A are on. Signals present at the O.W. XMT INPUT are passed through U3-A to the output amplifier. The output amplifier consists of R3 through R5, U1-A, R15, and R12. Potentiometer R12 provides a level adjustment range of +7 to -16dBm (with a nominal level of 0dBm at the O.W. XMT INPUT). The signal from the output amplifier goes to T1 which connects to the CH 6 XMT (pins 21 and 22) port.

4.2.19. The CH 6 RINGBACK SIGNAL IN (pin L) input consists of C1, C2, C36, R1, and R2. Signals present at this input are summed into the CH 6 XMT output.

4.3. O.W. RCV OUTPUT CIRCUITRY

4.3.1. The CH 1 RCV (pins M and N) input is terminated by R80. The input amplifier consists of R79, R81 through R85, R92, C19, C20, and U8-B. The output of U8-B connects to transmission gate U9-C.

4.3.2. When the CH 1 SEL. input is at -15VDC, Channel 1 and transmission gate U9-C are OFF.

4.3.3. When the CH 1 SEL. input is at GND, Channel 1 and transmission gate U9-C are on. Signals present at the CH 1 RCV input are passed through U9-C and are routed to the output summing amp (U10-B). Potentiometer R92 provides level adjustment to accommodate input levels from +7 to -16dBm (with a nominal level of 0dBm at the O.W. RCV OUTPUT).

4.3.4. The CH 2 RCV (pins P and R) input is terminated by R71. The input amplifier consists of R68, R69, R70, R72, R73, R76, R91, C17, C18, and U8-A. The output of U8-A connects to transmission gate U9-D.

4.3.5. When the CH 2 SEL. input is at -15VDC, Channel 2 and transmission gate U9-D are OFF.

4.3.6. When the CH 2 SEL. input is at GND, Channel 2 and transmission gate U9-D are on. Signals present at the CH 2 RCV input are passed through U9-D and are routed to the output summing amp (U10-B). Potentiometer R91 provides level adjustment to accommodate input levels from +7 to -16dBm (with a nominal level of 0dBm at the O.W. RCV OUTPUT).

4.3.7. The CH 3 RCV (pins S and T) input is terminated by R50. The input amplifier consists of R49, R51 through R55, R62, C12, C13, and U5-B. The output of U5-B connects to transmission gate U6-C.

4.3.8. When the CH 3 SEL. input is at -15VDC, Channel 3 and transmission gate U6-C are OFF.

4.3.9. When the CH 3 SEL. input is at GND, Channel 3 and transmission gate U6-C are on. Signals present at the CH 3 RCV input are passed through U6-C and are routed to the output summing amp (U10-B). Potentiometer R62 provides level adjustment to accommodate input levels from +7 to -16dBm (with a nominal level of 0dBm at the O.W. RCV OUTPUT).

4.3.10. The CH 4 RCV (pins U and V) input is terminated by R41. The input amplifier consists of R38, R39, R40, R42, R43, R46, R61, C10, C11, and U5-A. The output of U5-A connects to transmission gate U6-D.

4.3.11. When the CH 4 SEL. input is at -15VDC, Channel 4 and transmission gate U6-D are OFF.

4.3.12. When the CH 4 SEL. input is at GND, Channel 4 and transmission gate U6-D are ON. Signals present at the CH 4 RCV input are passed through U6-D and are routed to the output summing amp (U10-B). Potentiometer R61 provides level adjustment to accommodate input levels from +7 to -16dBm (with a nominal level of 0dBm at the O.W. RCV OUTPUT).

4.3.13. The CH 5 RCV (pins W and X) input is terminated by R18. The input amplifier consists of R17, R19 through R23, R30, C5, C6, and U2-B. The output of U2-B connects to transmission gate U3-C.

4.3.14. When the CH 5 SEL. input is at -15VDC, Channel 5 and transmission gate U3-C are OFF.

4.3.15. When the CH 5 SEL. input is at GND, Channel 5 and transmission gate U3-C are on. Signals present at the CH 5 RCV input are passed through U3-C and are routed to the output summing amp (U10-B). Potentiometer R30 provides level adjustment to accommodate input levels from +7 to -16dBm (with a nominal level of 0dBm at the O.W. RCV OUTPUT).

4.3.16. The CH 6 RCV (pins Y and Z) input is terminated by R9. The input amplifier consists of R6, R7, R8, R10, R11, R14, R29, C3, C4, and U2-A. The output of U2-A connects to transmission gate U3-D.

4.3.17. When the CH 6 SEL. input is at -15VDC, Channel 6 and transmission gate U3-D are OFF.

4.3.18. When the CH 6 SEL. input is at GND, Channel 6 and transmission gate U3-D are on. Signals present at the CH 6 RCV input are passed through U3-D and are routed to the output summing amp (U10-B). Potentiometer R29 provides level adjustment to accommodate input levels from +7 to -16dBm (with a nominal level of 0dBm at the O.W. RCV OUTPUT).

4.3.19. The output summing amplifier consists of R99 through R107 and U10-B. The output of U10-B connects to T7. The output of T7 connect to the O.W. RCV OUTPUT (pins 9 and 10).